TSL1401CL

128 × 1 Linear Sensor Array with Hold

General Description

The TSL1401CL linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and an internal pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The array is made up of 128 pixels, each of which has a photo-sensitive area of 3524.3 square micrometers. There is 8µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the TSL1401CL, Linear Sensor Array with Hold, are listed below:

Figure 1:
Added Value of Using TSL1401CL

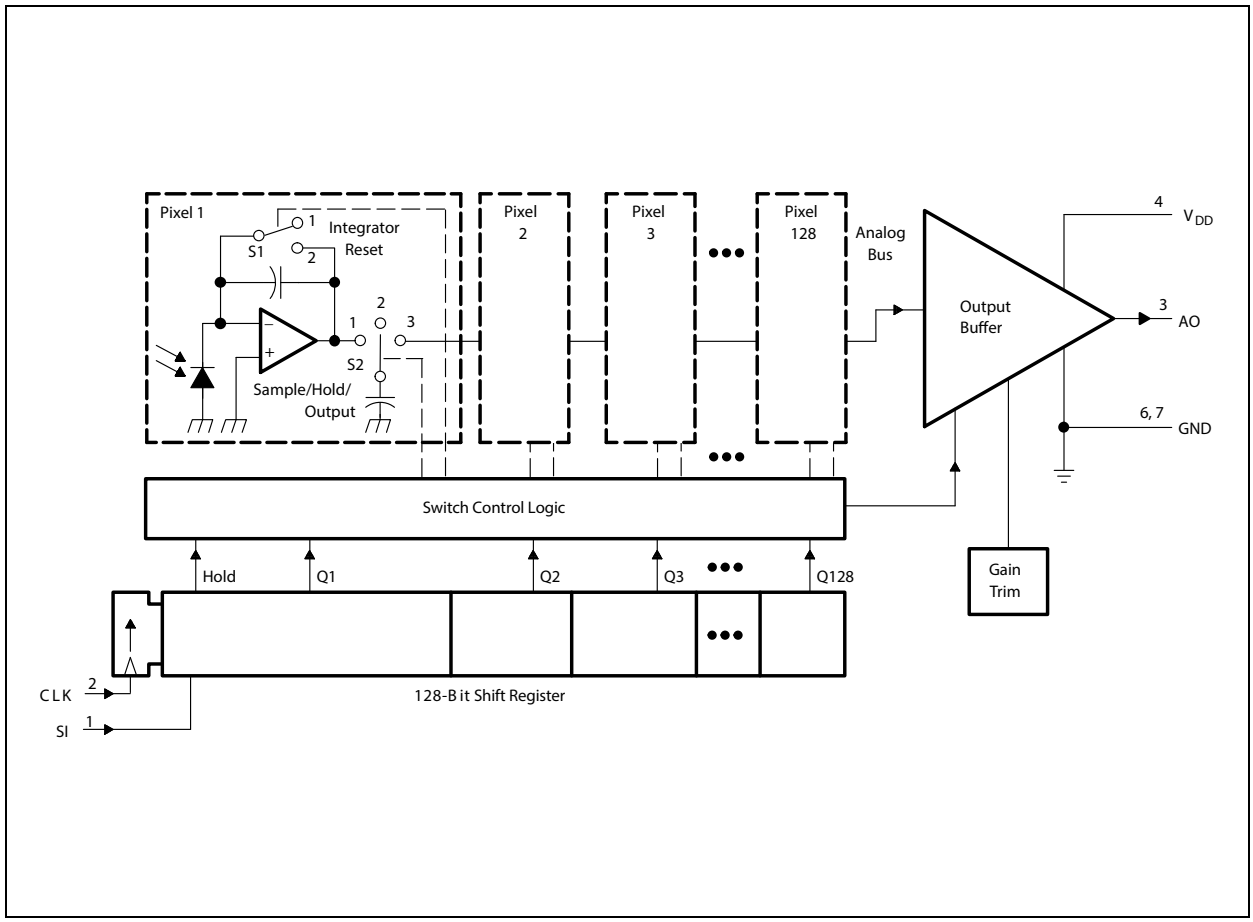
Benefits	Features
• Provides High Density Pixel Count	• 128 x 1 Sensor-Element Organization
• Enables High Resolution Scanning	• 400 Dots-Per-Inch (DPI) Sensor Pitch
• Enables Capacitive Threshold Sensing	• High Linearity and Uniformity
• Provides Full Dynamic Range	• Rail-to-Rail Output Swing (AO)

- Wide Dynamic Range... 4000:1 (72dB)
- Output Referenced to Ground
- Low Image Lag... 0.5% Typ
- Operation to 8MHz
- Single 3V to 5V Supply
- No External Load Resistor Required
- Replacement for TSL1401R-LF
- RoHS Compliant

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL1401CL Block Diagram



Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock. An internal signal, called Hold, is generated from the rising edge of SI and transmitted to analog switches in the pixel circuit. This causes all 128 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. Simultaneously, during the first 18 clock cycles, all pixel integrators are reset, and the next integration cycle begins on the 19^{th} clock. On the 129^{th} clock rising edge, the SI pulse is clocked out of the shift register and the analog output AO assumes a high impedance state. Note that this 129^{th} clock pulse is required to terminate the output of the 128^{th} pixel, and return the internal logic to a known state. If a minimum integration time is desired, the next SI pulse may be presented after a minimum delay of t_{qt} (pixel charge transfer time) after the 129^{th} clock pulse.

AO is an op amp-type output that does not require an external pull-down resistor. This design allows a rail-to-rail output voltage swing. With V_{DD} = 5V, the output is nominally 0V for no light input, 2V for normal white level, and 4.8V for saturation light level. When the device is not in the output phase, AO is in a high-impedance state.

The voltage developed at analog output (AO) is given by:

$V_{out} = V_{drk} + (R_e) (E_e) (t_{int})$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in $V/(\mu J/cm^2)$
- E_e is the incident irradiance in $\mu W/cm^2$
- t_{int} is integration time in seconds

A 0.1µF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

The TSL1401CL is intended for use in a wide variety of applications, including: image scanning, mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding.

Pin Assignments

The TSL1401CL pin assignments are described below:

Figure 3:
Pin Diagram

Pin Diagram:
NC - No internal connection
Package drawing is not to scale

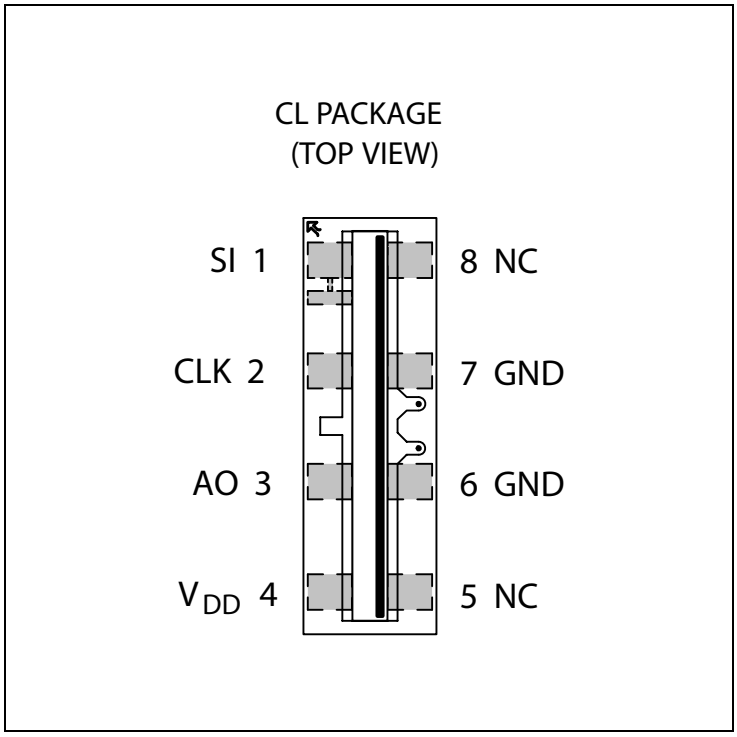


Figure 4:
Terminal Functions

Terminal		Description
Name	No.	
SI	1	Serial input. SI defines the start of the data-out sequence.
CLK	2	Clock. The clock controls charge transfer, pixel output, and reset.
AO	3	Analog output
V_{DD}	4	Supply voltage. Supply voltage for both analog and digital circuits.
NC	5, 8	No internal connection
GND	6, 7	Ground (substrate). All voltages are referenced to the substrate.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage range	-0.3	6	V
V_I	Input voltage range	-0.3	V_{DD} + 0.3V	V
I_{IK}	Input clamp current, (V_I < 0) or (V_I > V_{DD})	-20	20	mA
I_{OK}	Output clamp current, (V_O < 0) or (V_O > V_{DD})	-25	25	mA
V_O	Voltage range applied to any output in the high impedance or power-off state	-0.3	V_{DD} + 0.3V	V
I_O	Continuous output current, (V_O = 0 to V_{DD})	-25	25	mA
	Continuous current through V_{DD} or GND	-40	40	mA
I_O	Analog output current range	-25	25	mA
	Maximum light exposure at 638nm		5	mJ/cm^2
T_A	Operating free-air temperature range	-25	85	°C
T_{STRG}	Storage temperature range	-25	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions (see Figure 10 and Figure 11

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	3	5	5.5	V
V_I	Input voltage	0		V_{DD}	V
V_{IH}	High-level input voltage	2		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.8	V
λ	Wavelength of light source	400		1000	nm
f_{clock}	Clock frequency	5		8000	kHz
t_{int}	Sensor integration time (1)	0.03375		100	ms
$t_{su(SI)}$	Setup time, serial input	20			ns
$t_{h(SI)}$	Hold time, serial input (2)	0			ns
T_A	Operating free-air temperature	0		70	°C

Note(s):

1. Integration time is calculated as follows:
   $t_{int(min)}$ = (128 - 18) clock period + 20µs
   where *128* is the number of pixels in series, *18* is the required logic setup clocks, and *20µs* is the pixel charge transfer time (t_{qt})
2. SI must go low before the rising edge of the next clock pulse.

Figure 7:
Electrical Characteristics at f_{clock} = 1MHz, V_{DD} = 5V, T_A = 25°C, λ_p = 640nm, t_{int} = 5ms, R_L = 330Ω, E_e = 11µW/cm² (unless otherwise noted) (1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{out}	Analog output voltage (white, average over 128 pixels)	See note (2)	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)	E_e = 0	0	0.1	0.2	V
PRNU	Pixel response nonuniformity	See note (3)		±4%	±10%	
	Nonlinearity of analog output voltage	See note (4)		±0.4%		FS
	Output noise voltage	See note (5)		1		mVrms
R_e	Responsivity	See note (6)	25	35	45	V/(µJ/cm²)
V_{sat}	Analog output saturation voltage	V_{DD} = 5V, R_L = 330Ω	4.5	4.8		V
		V_{DD} = 3V, R_L = 330Ω	2.5	2.8		
SE	Saturation exposure	V_{DD} = 5V (7)		136		nJ/cm²
		V_{DD} = 3V (7)		78		
DSNU	Dark signal nonuniformity	All pixels, E_e = 0 (8)		0.02	0.05	V
IL	Image lag	See note (9)		0.5%		
I_{DD}	Supply current	V_{DD} = 5V, E_e = 0		2.8	4.5	mA
		V_{DD} = 3V, E_e = 0		2.6	4.5	
I_{IH}	High-level input current	$V_I = V_{DD}$			1	µA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{IL}	Low-level input current	$V_I = 0$			1	µA
C_i	Input capacitance			5		pF

Note(s):

1. All measurements made with a 0.1µF capacitor connected between V_{DD} and ground.
2. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640nm.
3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. $R_{e(min)} = [V_{out(min)} - V_{drk(max)}] \div (E_e \times t_{int})$
7. $SE_{(min)} = [V_{sat(min)} - V_{drk(min)}] \times (E_e \times t_{int}) \div [V_{out(max)} - V_{drk(min)}]$
8. DSNU is the difference between the maximum and minimum output voltage for all pixels in the absence of illumination.
9. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out(IL)} - V_{drk}}{V_{out(white)} - V_{drk}} \times 100$$

Figure 8:
Timing Requirements (see Figure 10 and Figure 11)

Symbol	Parameter	Min	Nom	Max	Unit
$t_{su(SI)}$	Setup time, serial input (1)	20			ns
$t_{h(SI)}$	Hold time, serial input (1), (2)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns
t_{qt}	Pixel charge transfer time	20			µs

Note(s):

1. Input pulses have the following characteristics: t_r = 6ns, t_f = 6ns.
2. SI must go low before the rising edge of the next clock pulse.

Figure 9:
Dynamic Characteristics over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_s	Analog output settling time to ±1%	R_L = 330Ω, C_L = 10pF		120		ns

Parameter Measurement Information

Figure 10:
Timing Waveforms

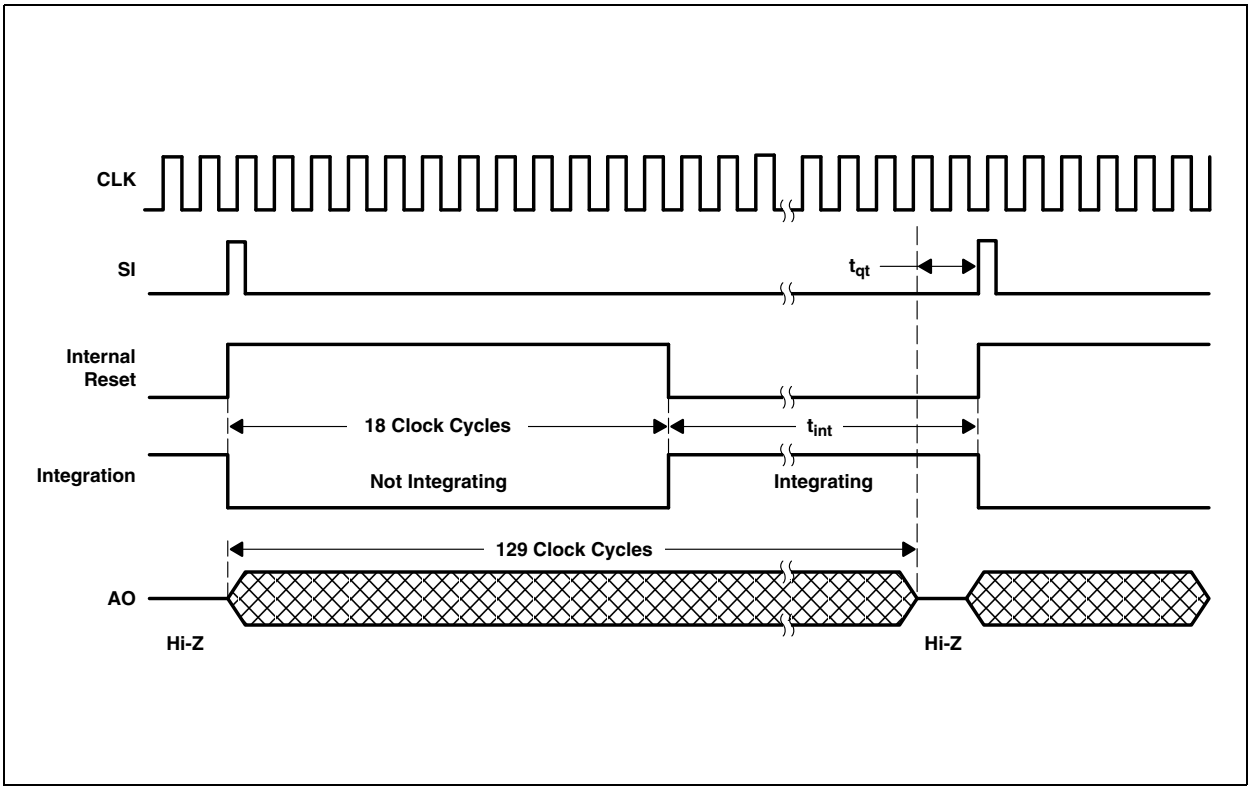
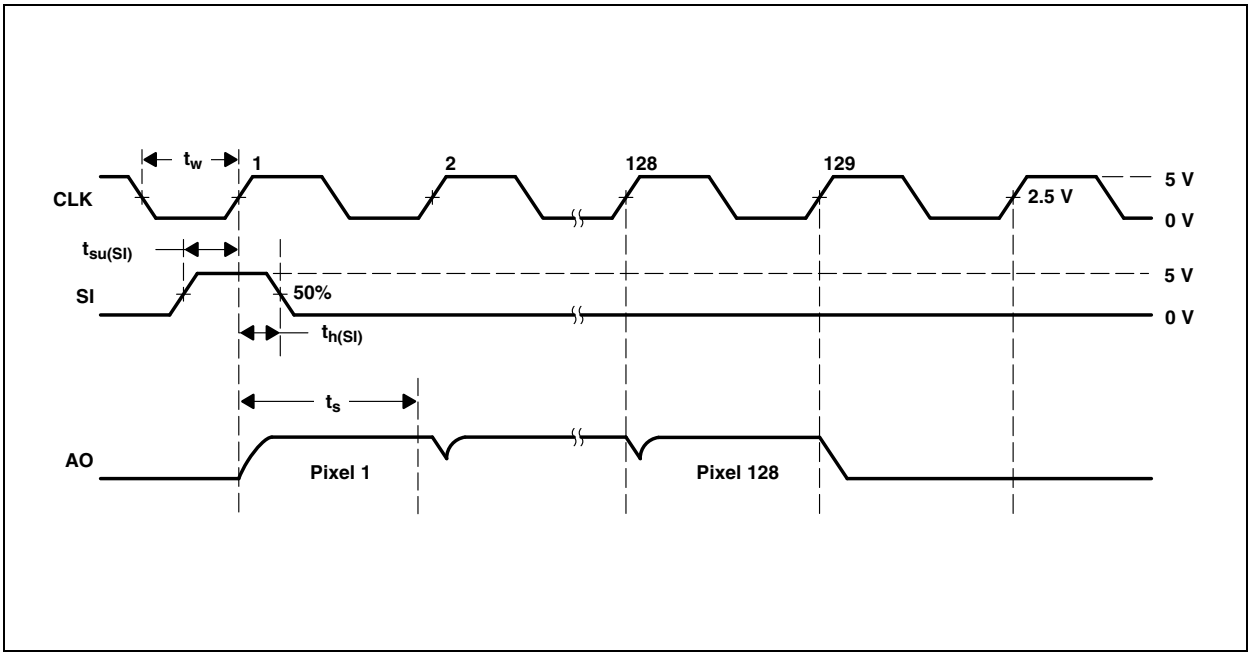


Figure 11:
Operational Waveforms



Typical Characteristics

Figure 12:
Photodiode Spectral Responsivity

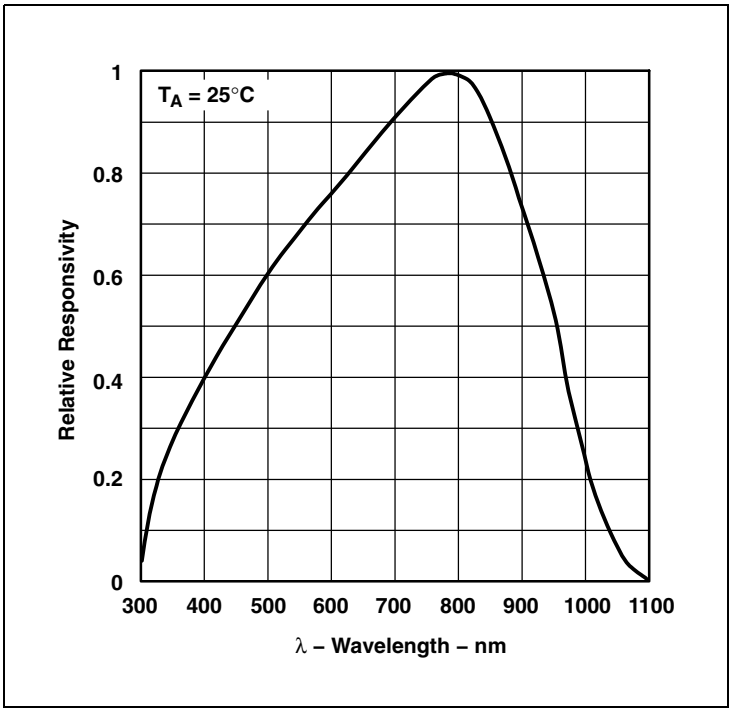


Figure 13:
Normalized Idle Supply Current vs. Free-Air Temperature

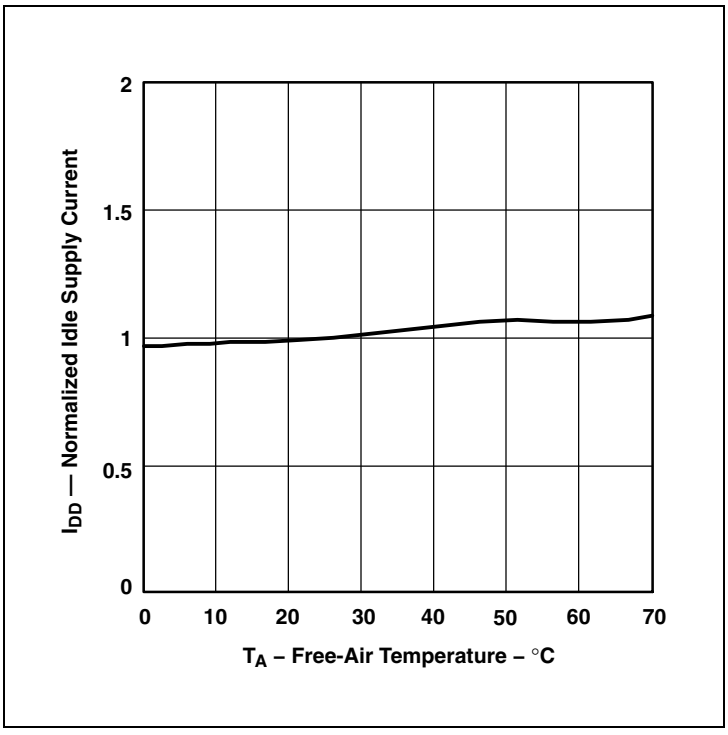


Figure 14:
White Output Voltage vs. Free-Air Temperature

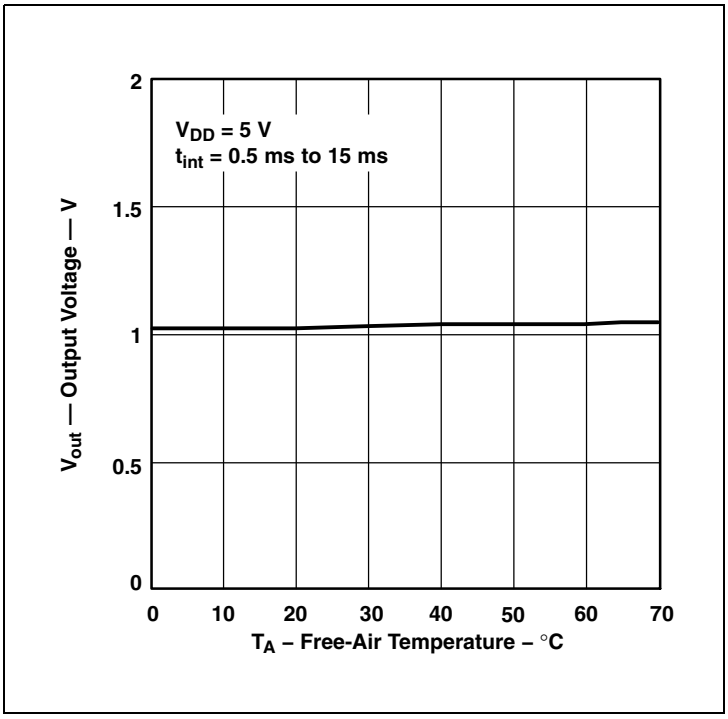


Figure 15:
Dark Output Voltage vs. Free-Air Temperature

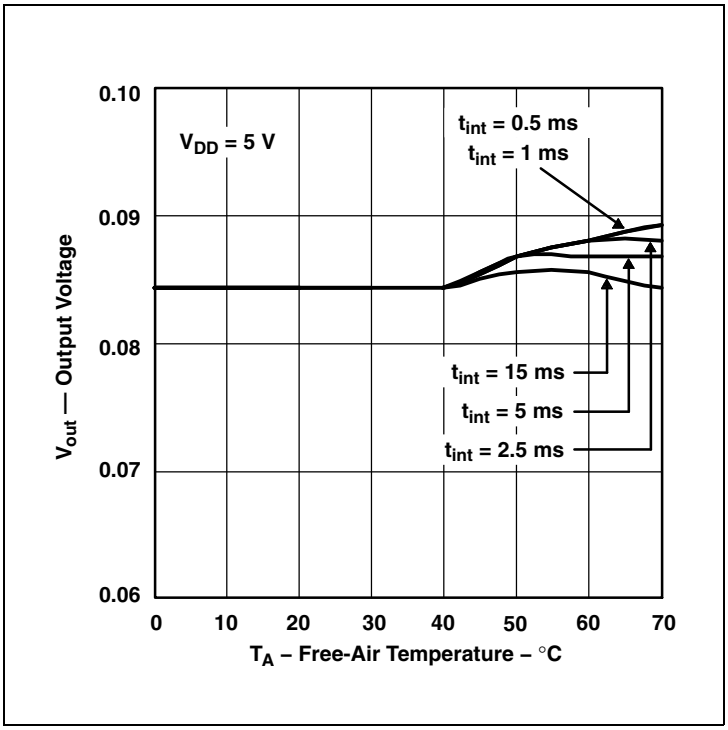


Figure 16:
Settling Time vs. Load (V_{DD}=3V)

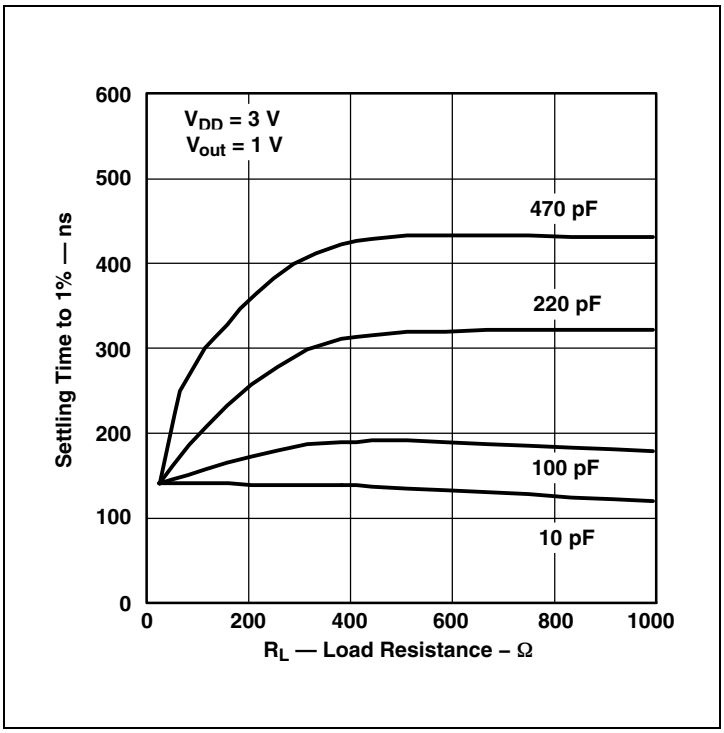
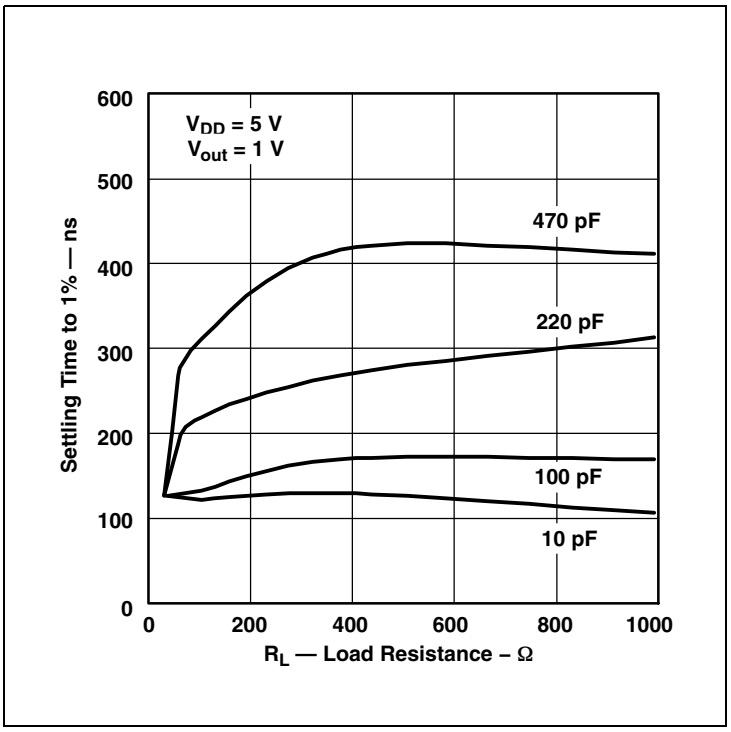


Figure 17:
Settling Time vs. Load (V_{DD}=5V)



Principles of Operation

Integration Time

The integration time of the linear array is the period during which light is sampled and charge accumulates on each pixel's integrating capacitor. The flexibility to adjust the integration period is a powerful and useful feature of the ams TSL14xx linear array family. By changing the integration time, a desired output voltage can be obtained on the output pin while avoiding saturation for a wide range of light levels.

The integration time is the time between the SI (Start Integration) positive pulse and the HOLD positive pulse minus the 18 setup clocks. The TSL14xx linear array is normally configured with the SI and HOLD pins tied together. This configuration will be assumed unless otherwise noted. Sending a high pulse to SI (observing timing rules for setup and hold to clock edge) starts a new cycle of pixel output and integration setup. However, a minimum of (n+1) clocks, where n is the number of pixels, must occur before the next high pulse is applied to SI. It is not necessary to send SI immediately on/after the (n+1) clocks. A wait time adding up to a maximum total of 100ms between SI pulses can be added to increase the integration time creating a higher output voltage in low light applications.

Each pixel of the linear array consists of a light-sensitive photodiode. The photodiode converts light intensity to a voltage. The voltage is sampled on the Sampling Capacitor by closing switch S2 (position 1) (see Figure 2). Logic controls the resetting of the Integrating Capacitor to zero by closing switch S1 (position 2).

At SI input, all of the pixel voltages are simultaneously scanned and held by moving S2 to position 2 for all pixels. During this event, S2 for pixel 1 is in position 3. This makes the voltage of pixel 1 available on the analog output. On the next clock, S2 for pixel 1 is put into position 2 and S2 for pixel 2 is put into position 3 so that the voltage of pixel 2 is available on the output.

Following the SI pulse and the next 17 clocks after the SI pulse is applied, the S1 switch for all pixels remains in position 2 to reset (zero out) the integrating capacitor so that it is ready to begin the next integration cycle. On the rising edge of the 19^{th} clock, the S1 switch for all the pixels is put into position 1 and all of the pixels begin a new integration cycle.

The first 18 pixel voltages are output during the time the integrating capacitor is being reset. On the 19^{th} clock following an SI pulse, pixels 1 through 18 have switch S2 in position 1 so that the sampling capacitor can begin storing charge. For the period from the 19^{th} clock through the n^{th} clock, S2 is put into position 3 to read the output voltage during the n^{th} clock. On the next clock the previous pixel S2 switch is put into position 1

to start sampling the integrating capacitor voltage. For example, S2 for pixel 19 moves to position 1 on the 20th clock. On the *n*+1 clock, the S2 switch for the last (*n*th) pixel is put into position 1 and the output goes to a high-impedance state.

If a SI was initiated on the *n*+1 clock, there would be no time for the sampling capacitor of pixel *n* to charge to the voltage level of the integrating capacitor. The minimum time needed to guarantee the sampling capacitor for pixel *n* will charge to the voltage level of the integrating capacitor is the charge transfer time of 20µs. Therefore, after *n*+1 clocks, an extra 20µs wait must occur before the next SI pulse to start a new integration and output cycle.

The minimum integration time for any given array is determined by time required to clock out all the pixels in the array and the time to discharge the pixels. The time required to discharge the pixels is a constant. Therefore, the minimum integration period is simply a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time and reduces the maximum light level for saturation on the output. The minimum integration time shown in this data sheet is based on the maximum clock frequency of 8MHz.

The minimum integration time can be calculated from the equation:

$$T_{int(min)} = \left(\frac{1}{\text{maximum clock frequency}}\right) \times (n - 18)\text{pixels} + 20\mu s$$

where:

n is the number of pixels

In the case of the TSL1401CL with the maximum clock frequency of 8MHz, the minimum integration time would be:

$T_{int(min)} = 0.125\mu s \times (128 - 18) + 20\mu s = 33.75\mu s$

It is good practice on initial power up to run the clock (*n*+1) times after the first SI pulse to clock out indeterminate data from power up. After that, the SI pulse is valid from the time following (*n*+1) clocks. The output will go into a high-impedance state after the *n*+1 high clock edge. It is good practice to leave the clock in a low state when inactive because the SI pulse required to start a new cycle is a low-to-high transition.

The integration time chosen is valid as long as it falls in the range between the minimum and maximum limits for integration time. If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. If this occurs, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling

window is active is to lower the output voltage level to prevent saturation. However, the integration time must still be greater than or equal to the minimum integration period.

If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the integrating capacitors on the pixels can hold their accumulated charge. The maximum integration time should not exceed 100ms for accurate measurements.

It should be noted that the data from the light sampled during one integration period is made available on the analog output during the next integration period and is clocked out sequentially at a rate of one pixel per clock period. In other words, at any given time, two groups of data are being handled by the linear array: the previous measured light data is clocked out as the next light sample is being integrated.

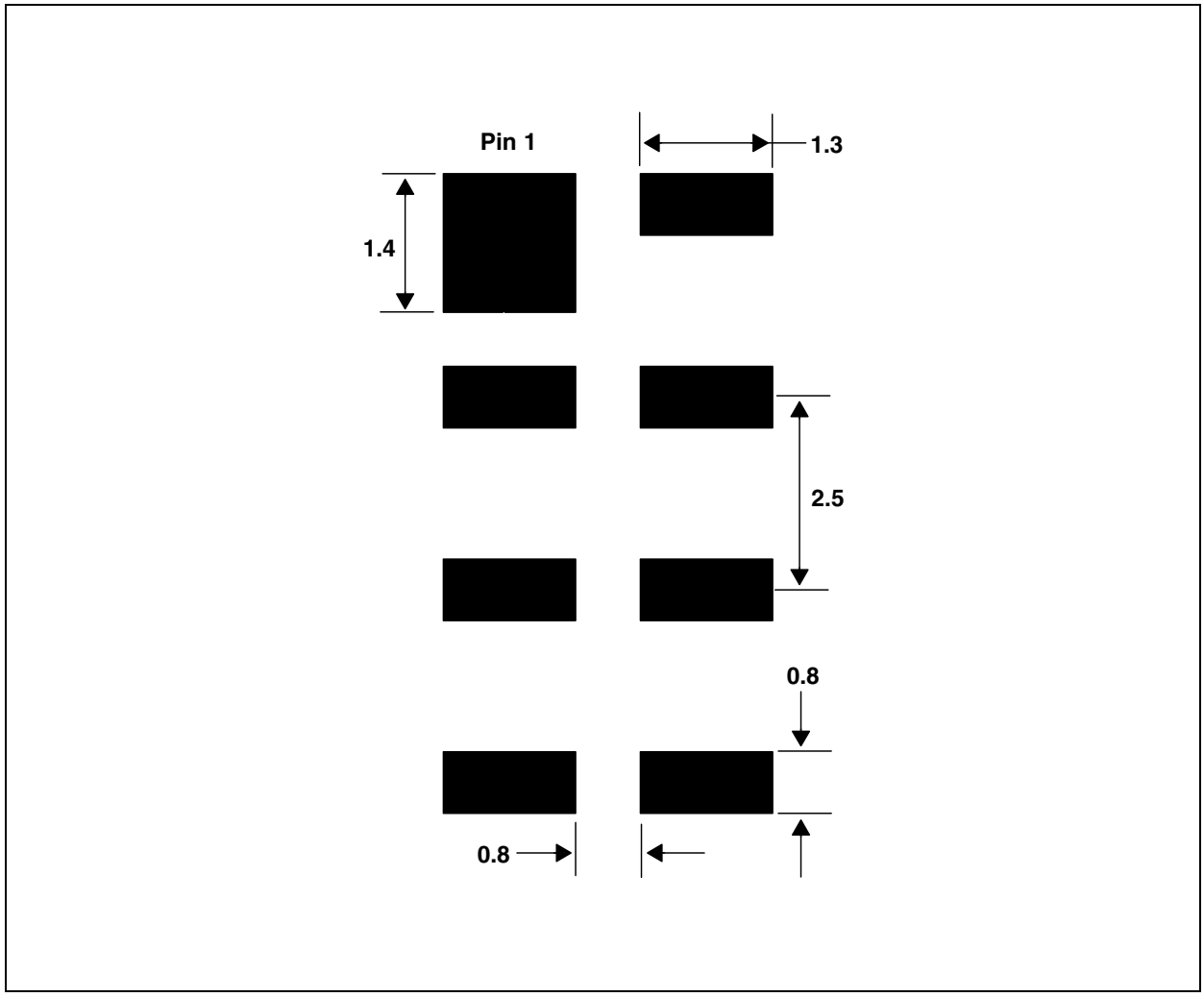
Although the linear array is capable of running over a wide range of operating frequencies up to a maximum of 8MHz, the speed of the A/D converter used in the application is likely to be the limiter for the maximum clock frequency. The voltage output is available for the whole period of the clock, so the setup and hold times required for the analog-to-digital conversion must be less than the clock period.

Application Information: Hardware

PCB Pad Layout

Suggested PCB pad layout guidelines for the CL package are shown in Figure 18.

Figure 18:
Suggested CL Package PCB Layout

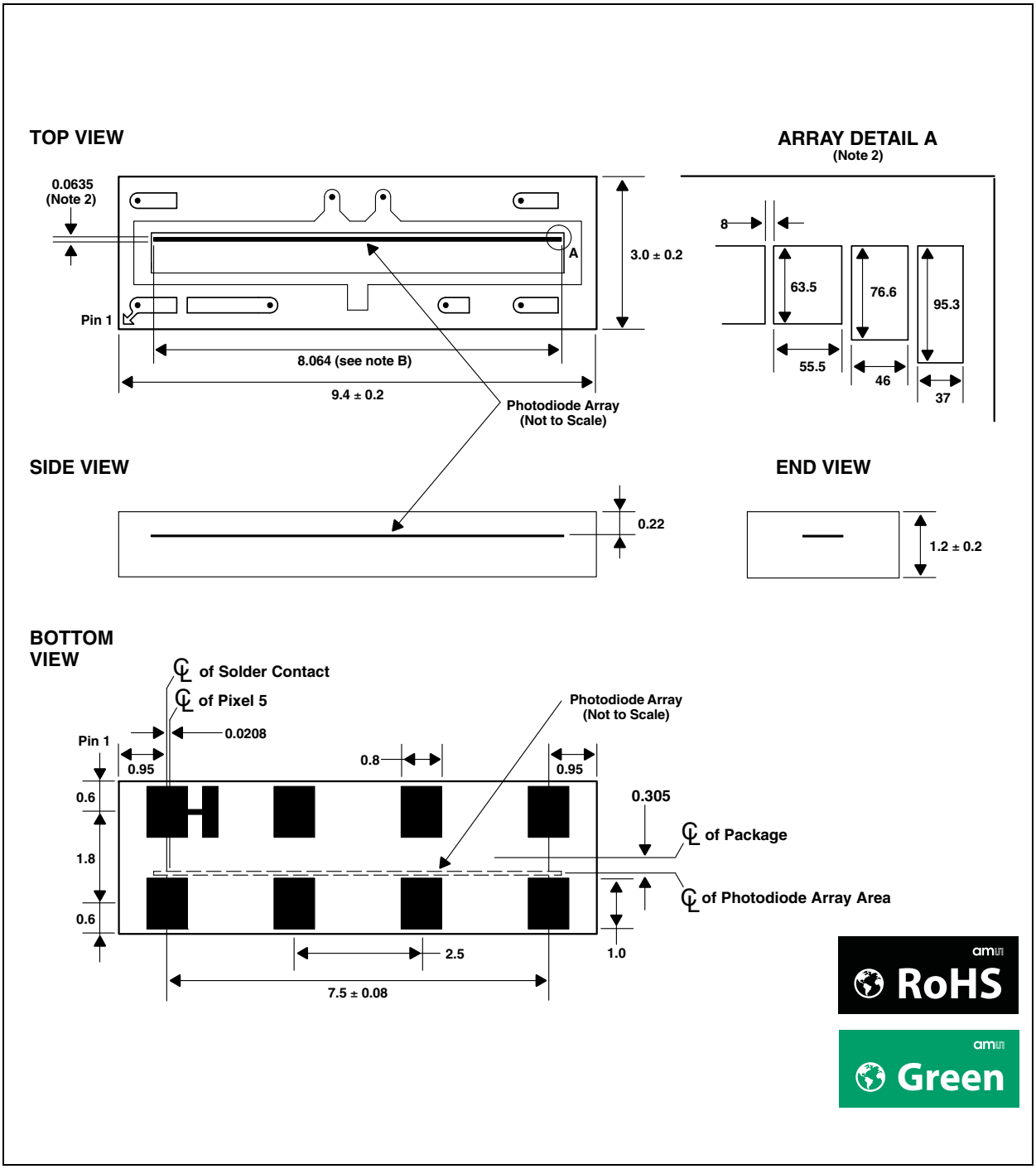


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Information

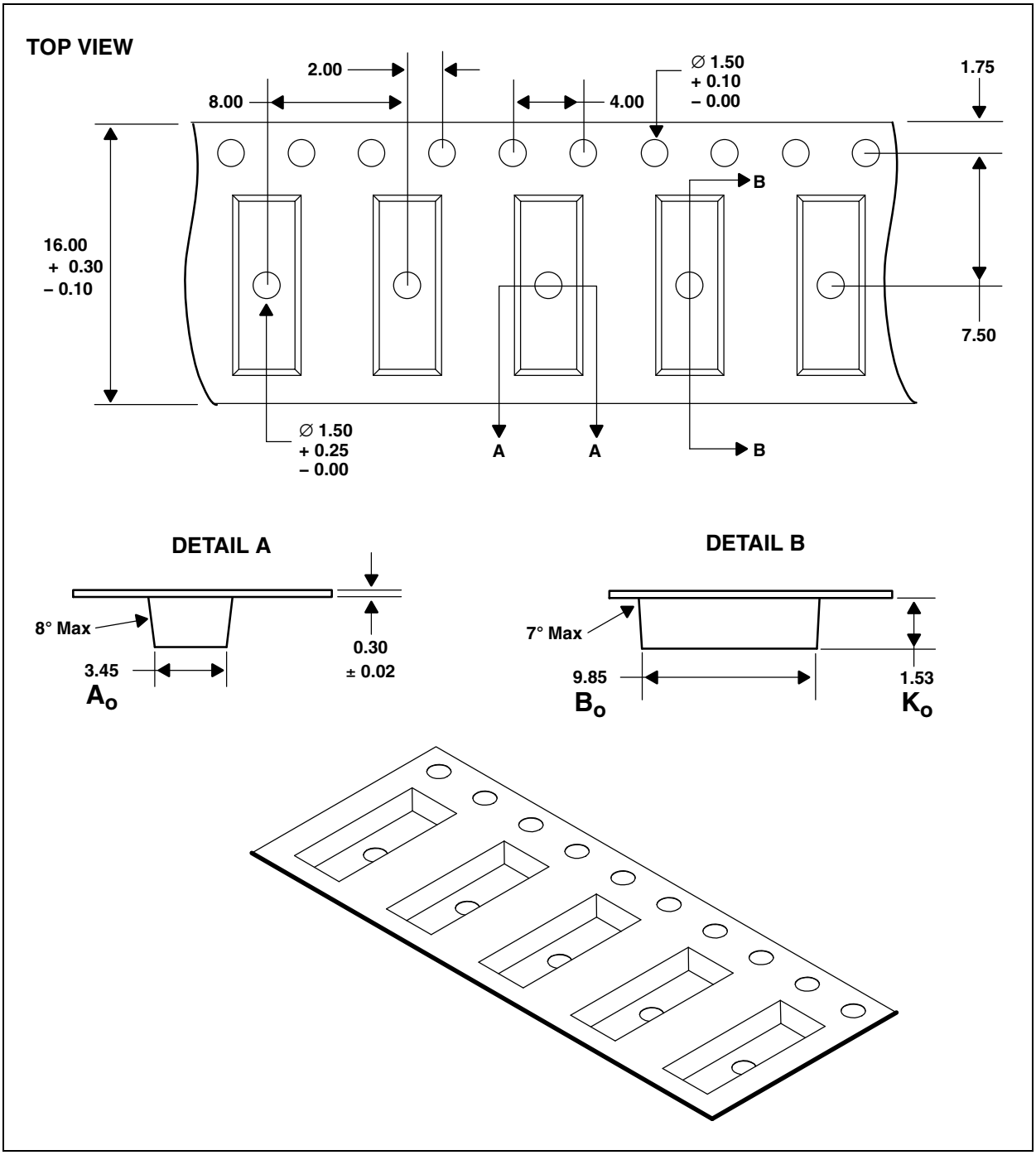
Figure 19:
Package CL Configuration



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.05mm unless otherwise noted.
2. Nominal photodiode array dimension. The array is made up of 124 inner pixels, 2 next-to-end pixels, and 2 end pixels. Pixel #1 is closer to Pin 1. The inner pixels measure 63.5µm (H) by 55.5µm (W), the next-to-end pixels are 76.6µm (H) by 46µm (W), and the end pixels are 95.3µm (H) by 37µm (W). There is 8µm spacing between all pixels. See Array Detail A.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.56.
4. Contact finish is soft gold plated.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Figure 20:
Package CL Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 1000 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering Information

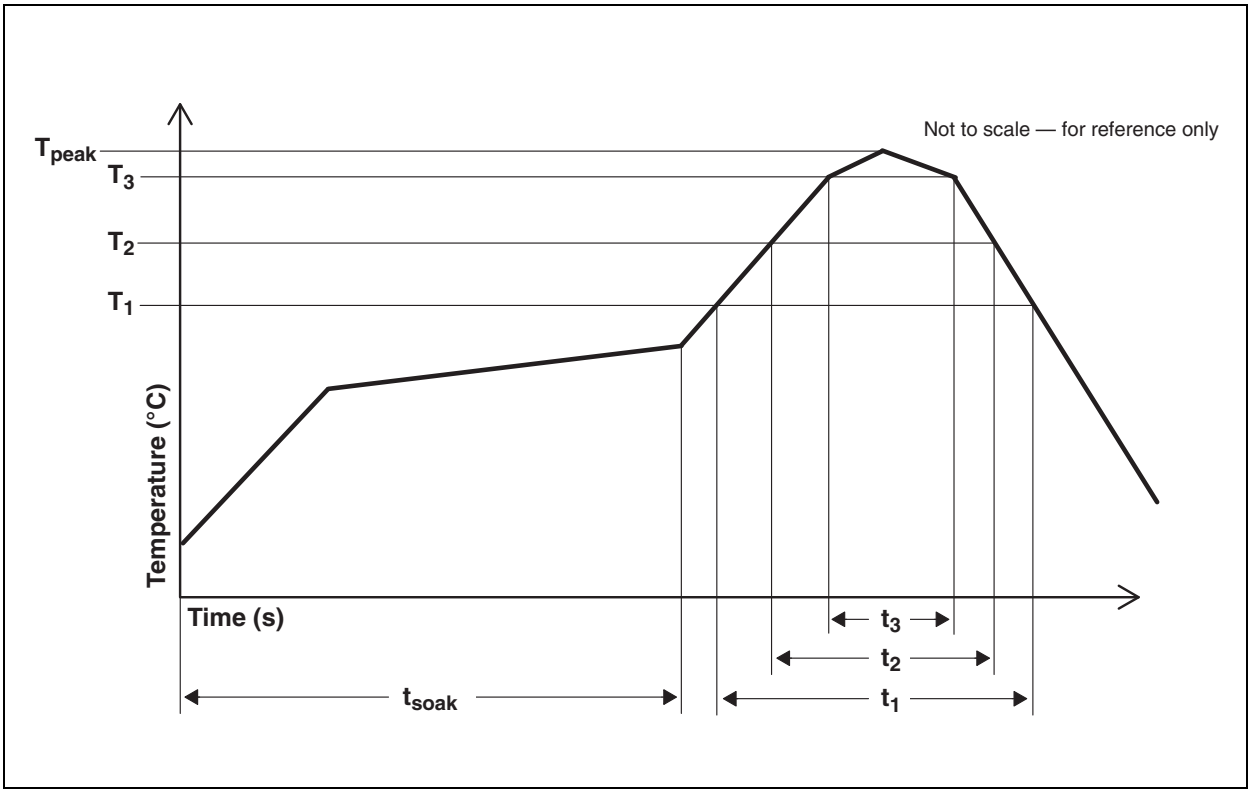
The CL package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 21:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above T_{peak} - 10°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max -5°C/s

Figure 22:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The CL package has been assigned a moisture sensitivity level of MSL 5a and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 6 months from the date code on the aluminized envelope - if unopened
- Opened Time: 24 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 24 hours. If rebaking is required, it should be done at 60°C for 24 hours.

Ordering & Contact Information

Figure 23:
Ordering Information

Ordering Code	Type	Package Designator	Delivery Form	Delivery Quantity
TSL1401CL	128 × 1 Array	CL	Tape & Reel	1000 pcs/reel

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RoHS Compliant & ams Green Statement

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ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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Revision Information

Changes from 1-00 (2016-Jun-21) to current revision 1-01 (2017-Aug-30)	Page
Updated Figure 5 and removed notes under it	6

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide